The way to securely design a low-power SoC demonstrated on Silicon

Dolphin Integration

ABSTRACT

Designing right-on-first-pass an ultra low-power SoC made of multiple power domains, while meeting noise propagation and mode transition performance constraints, is a major challenge for any SoC integrator but is mandatory to reach its market on time for any Fabless.

This presentation will first review some of the often not understood and overlooked difficulties to be overcome for the design of an ultra low-power SoC. It will then present a breakthrough methodology for the rigorous construction of a SoC taking into account low-power starting from the architecture definition and all along the design flow. Such a breakthrough methodology enables to safely minimize power consumption and silicon area by avoiding oversized power regulation networks while taking BoM cost constraints into account.

Proven on silicon through a demochip in TSMC 55 nm uLP with dynamical tests involving multiple Silicon IPs representative of expected interactions, this methodology gives full confidence to Silicon IP users that designing an ultra-low power SoC is safely tractable.

Identified and validated in the frame of the demochip, new deliverables, enabling users of Silicon IPs to succeed confidently and cost-effectively their design of low-power SoCs, will be presented. The correlation of the demochip measurements with simulation results will illustrate the robustness of the methodology and highlight the added value to standard low-power flows using low-power TSMC technologies.

DOLPHIN INTEGRATION
The Enabler of Low-Power Systems-on-Chip

The way to securely design a low-power SoC demonstrated on Silicon

TSMC OIP 2016 – SAN JOSE

Not just a supplier of Technology, but provider of the Dolphin Integration **know-how**!

OVERVIEW

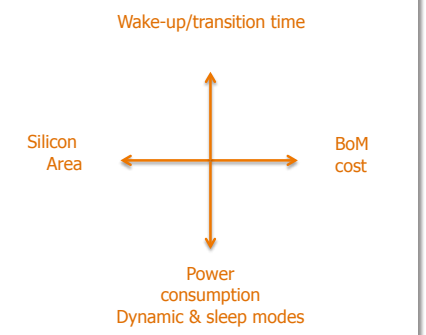
- IoT SoC context
- Ultra low-power SoC design challenges
- Methodology for rigorous construction of a SoC
- Fabric IP to make the hard easy
- Additional verifications for hot spots
- Point product EDA solution
- Proven on silicon through a demochip
- Silicon correlation with Taishan illustrates robustness and added-value in 55 nm uLPeF
- Conclusion

IOT SOC CONTEXT

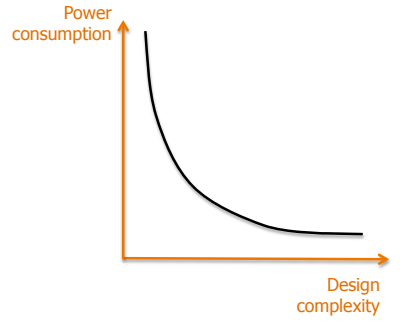
- IoT and wearable devices are battery powered
  - Battery life-time depends on the power consumption of the device
    - Low power consumption is required to increase battery life
- Need for efficient sleeping
  - Battery powered devices sleeping 99 % and active 1 %
- Need for efficient idling to reduce power and heating
  - Wall plug powered household devices waiting for user input
  - Wall plug powered network devices waiting for network traffic

WHY IS LOW-POWER A CHALLENGE?

Multi-dimension performance trade-off for a targeted speed



Trade-off



Low-Power Design Choices

- Partitioning a SoC into power domains is an effective technique to reduce both dynamic and leakage power

Process selection

Clock gating

Global power gating — UPF/CPF preferable

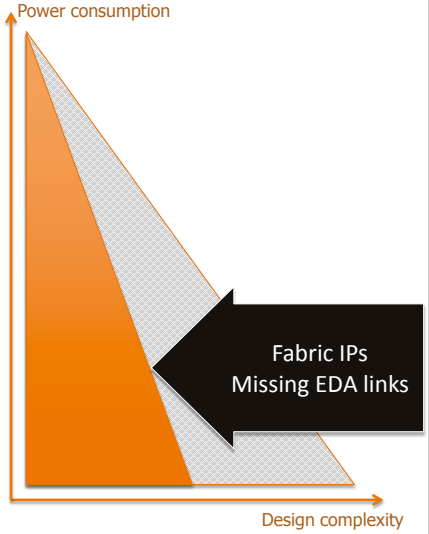
Coarse grain power gating — UPF/CPF required

Dynamic voltage and frequency stepping — UPF/CPF required

Minimizing power consumption while maintaining:
- Small silicon area
- Low BoM cost
- Fast Time-to-Market

New Challenges with Power Domains

- Budgeting power consumption at architectural level and refining down-to silicon
  - Efficiency of the SoC from a power consumption point-of-view (≠ regulator efficiency)
  - Risk of noise propagation vs. optimizing the number of regulators
- Describing power intent all along the design flow (UPF/CPF)
  - Power hierarchy (UPF) vs. functional hierarchy (RTL)
- Controlling power islands, their regulators and clock generators
  - Risk of incoherent startup state (default startup state)
- Mastering in-rush current when turning on power islands
  - Pairing vs. in-rush current
- Handling the always-on domain
  - Always supplied vs. always active
- Implementing scan mode vs. voltage regulators, clock generators…
- …



Methodology for Construction of a SoC

Process & input voltages

1 **Definition of SoC functional blocks**
Assemble the system or data bus for interactions between functions

Targeted performances
- *Main challenges*
- *Noise sensitivities*

2 **Identification of operating frequencies**
Determine frequency constraints of each block to distribute clocks

Identification of SoC power modes for partitioning in power domains
- *Power state table & activity scenario*

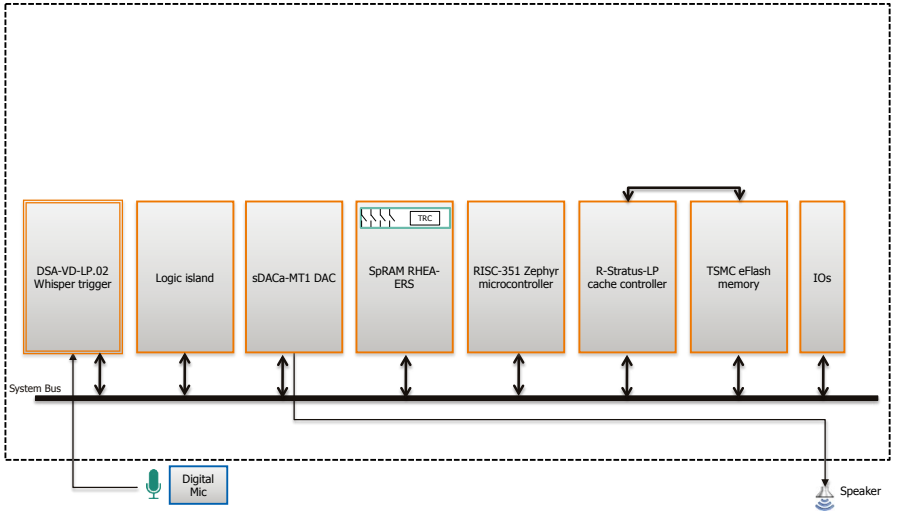
3 **Definition of the Power Regulation Network**
Group functions into power islands and assemble the power supply network depending on power and clock domains

Specification of the Activity Control Unit
- *Transition time requirements*

4 **Identification of the control network & definition of mode change sequences**
Handle mode transitions of power islands and control voltage regulators

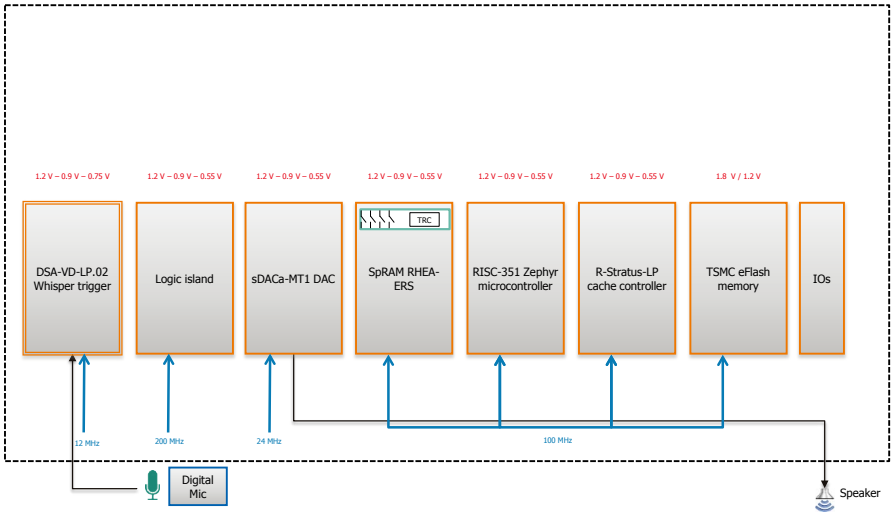
5 **Identification of Application Schematics**

SoC Functional Blocks (1/6)



- TRC – Transition Ramp Cell: control of the start-up of power sequence

Operating Frequencies & Voltages (2/6)



- TRC – Transition Ramp Cell: control of the start-up of power sequence

Power Domains (3/6)

CLICK
For a simplified and secured power gating management

Make it easy thanks to **CLICK**:

- Create power islands **whatever their contents**
- Handle **safely** and **automatically** the trade-off between wake-up time and in-rush current, thanks to the *Transition Ramp Controller*
- **Avoid oversized margins** and **design** iterations by construction thanks to the associated scripts and documentation

- RAR - Retention Alternating Regulator, combining regulators optimized for retention mode
- TRC – Transition Ramp Cell: control of the start-up of power sequence

Power Regulation Network (4/6)

DELTA – Reusable Power Kit Library
For a simplified, secured and optimized power regulation network

Make it possible thanks to the **DELTA Standard**, which is essential for:

- **Avoiding iterative design loops**
- Securing SoC integration by **ensuring the safe matching** of the regulators with their loads.
- **Easing the reuse** of voltage regulators and architectures.
- Allowing **best optimizations** for meeting each SoC challenges (high efficiency, low noise, low BoM, low leakage, high density)

- RAR - Retention Alternating Regulator, combining regulators optimized for retention mode
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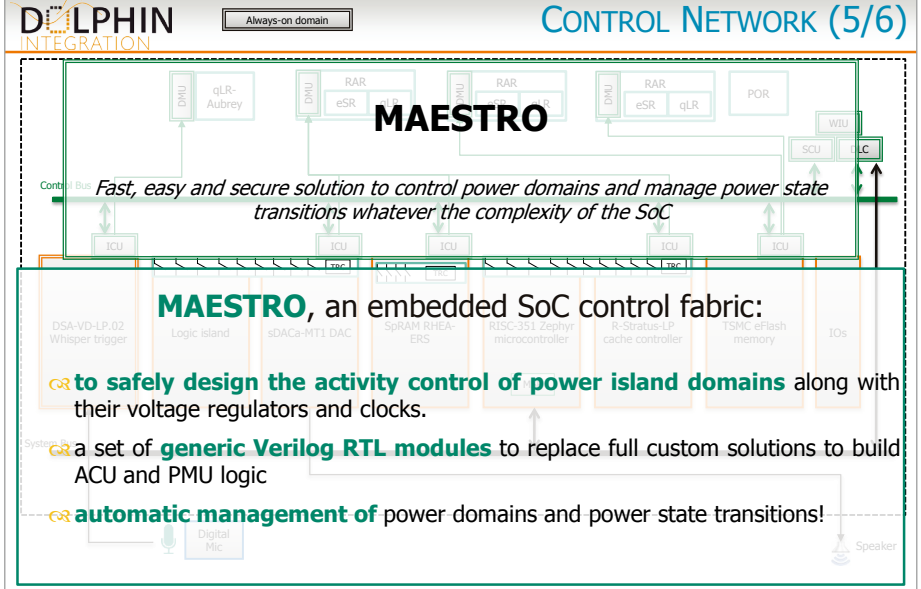
Control Network (5/6)

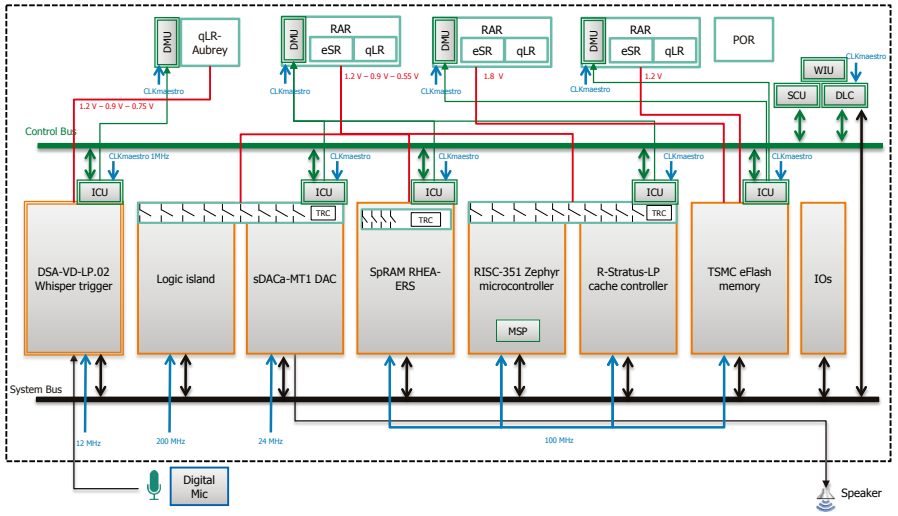


MAESTRO, an embedded SoC control fabric:

- **to safely design the activity control of power island domains** along with their voltage regulators and clocks.
- a set of **generic Verilog RTL modules** to replace full custom solutions to build ACU and PMU logic
- **automatic management of** power domains and power state transitions!

- RAR - Retention Alternating Regulator, combining regulators optimized for retention mode
- TRC – Transition Ramp Cell: control of the start-up of power sequence

Complete Networks (6/6)



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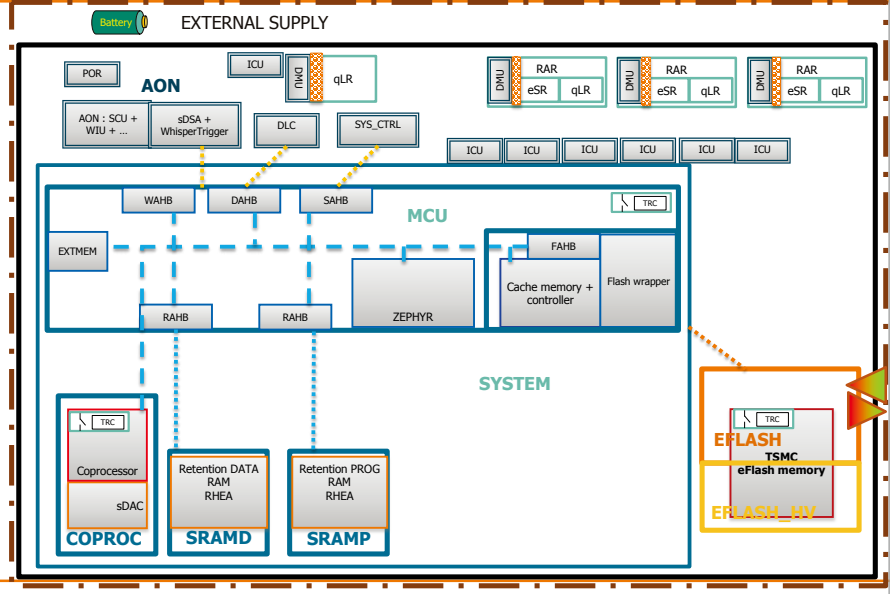
Power Regulation Network (UPF/CPF)



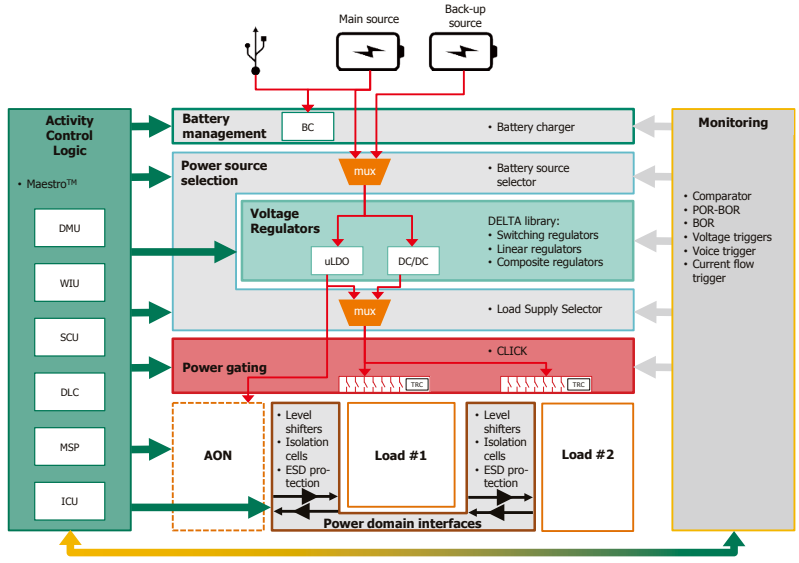
Ultra Low-Power Design Challenges

- Securing the implementation of a low-power SoC
  - By optimizing the number of power domains
  - By selecting the best Power Regulation Network
  - By simplifying the control of the power domains
  - By securing the power gating implementation
    - Inserting power switches and minimizing the loopbacks to floorplan
  - By enabling the functional and electrical verifications
    - Checking the transitions between power modes

Demonstrated with TAISHAN Demochip

Managing the design of a low-power SoC and then reducing the overall design complexity!

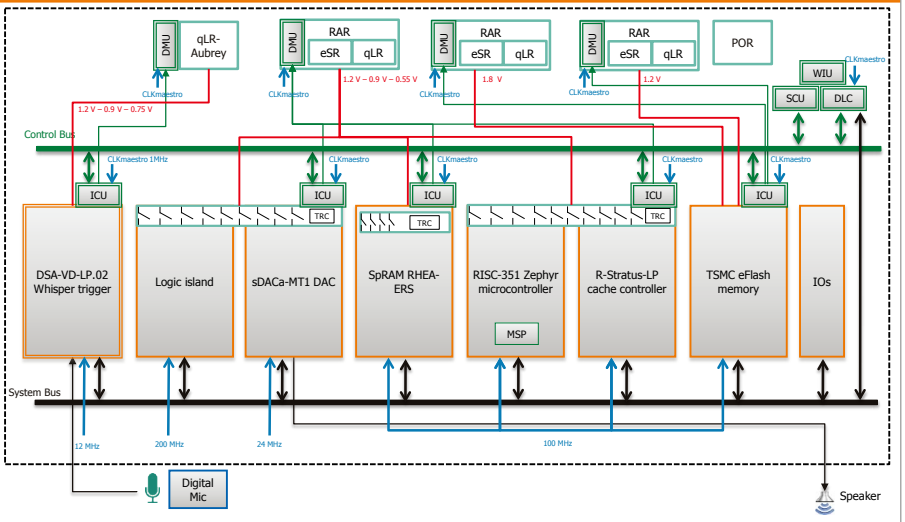
Fabric IP to make the hard easy



WHY ARE ADDITIONAL VERIFICATIONS REQUIRED?

- The industry is still in a handcrafted approach dominated by integration guidelines, margins and spreadsheets for integrating analog IPs in a SoC
  - Reaching limits of manageable complexity, error prone, longer design cycles, …
- System exploration is required to design competitive architectures for innovative products
  - Applying metrics with Figures-of-Merit (FoM)
- Power consumption is not power noise
  - Optimizing one may make the other worse!
- Need to check the pairing between regulators and their loads
  - Improving reliability
  - Securing the analog IPs performances
  - Optimizing SoC power efficiency with the best density

HOT SPOTS



- RAR - Retention Alternating Regulator, combining regulators optimized for retention mode
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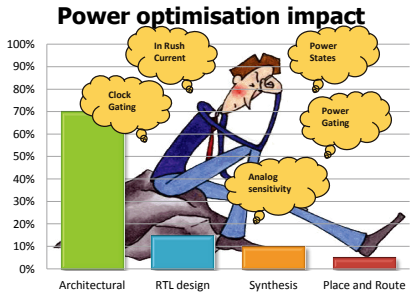
BUDGET EARLY & CHECK REGULARLY

- A budget-based approach
  - Secure integration of analog IPs
  - Optimize the area and the power at system level
  - Track design performance up to tape-out
- Early decisions at architectural level
  - Assess design trade-offs at an early stage
  - Save time, area and power thanks to a library of generic behavioral models and a methodology to check the hot spots
- Secure integration
  - Refine the same behavioral models all along the design flow
- Template/profile based methodology
  - Avoid the need to model the functionality of analog or RF loads



PowerVision™ EDA solution for

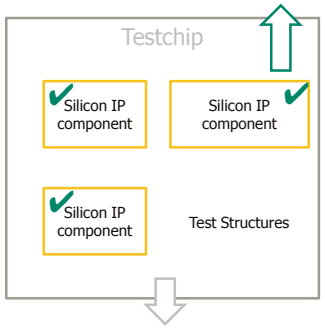
*Mode Transition Checks (**MTC**)*
&
*Noise Propagation Checks (**NPC**)*

NEW DELIVERABLES

- Unique specifications to check whether performances of regulators are preserved

Proven on Silicon through a DemoChip

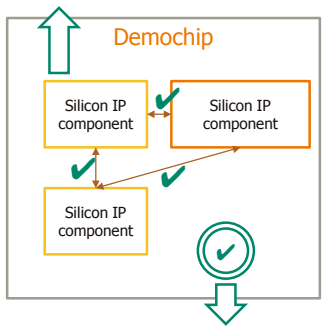
Qualification per foundry procedure



Silicon Measurement Report

VS

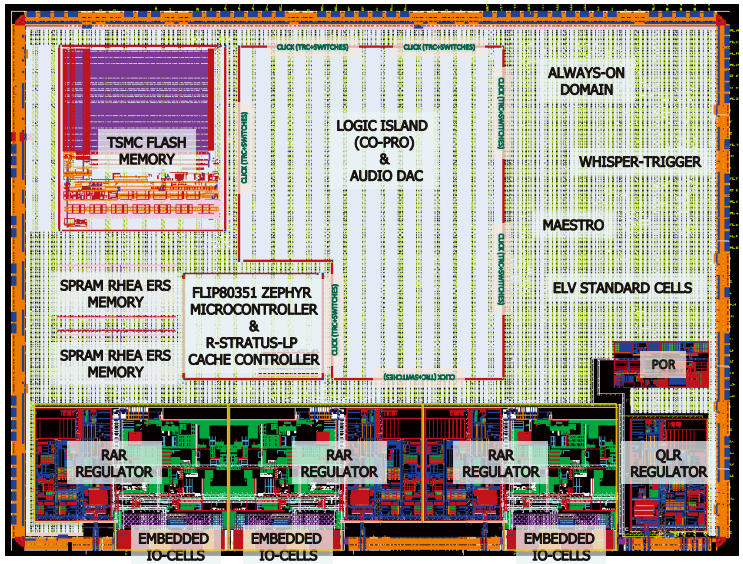
Dynamic interplay in the context of a SoC



Overall SoC architecture proven by dynamic tests involving multiple components

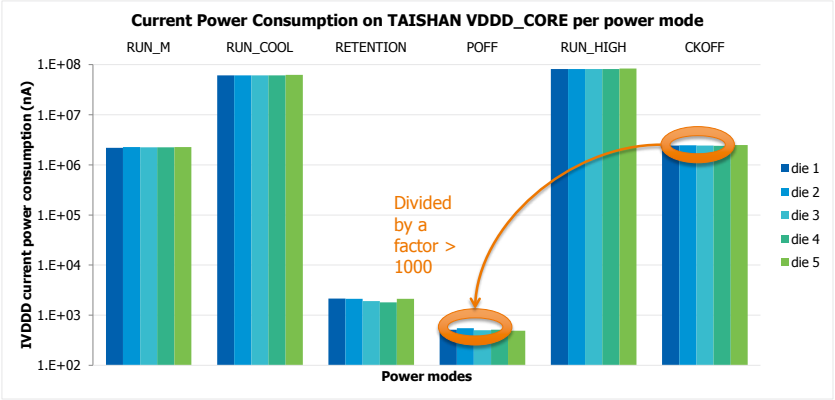
- TaiShan demochip for low-power SoC at TSMC 55 nm uLP eFlash
  - Characterizing the power mode switching performances when individual components are triggered-on and turned-off
  - Assessing the low-power SoC integration flow upgrades to succeed design and implementation

TaiShan DemoChip
12 mm² TSMC 55 nm eFlash



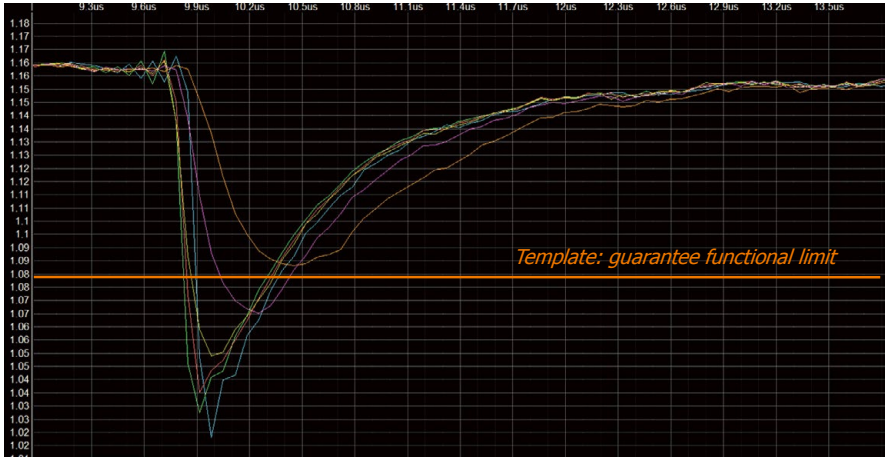
Silicon Correlation of Wake-up

- Wake-up a system from a sleep mode (extinction or retention) to an active mode without transition impact

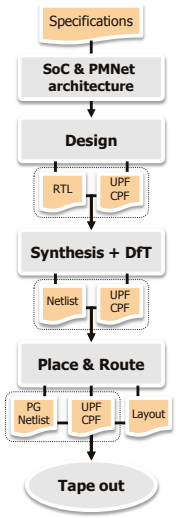


Silicon Correlation of In-rush Current

- Tune the in-rush current of power island keeping power integrity
  - Voltage drop according to different TRC settings



Low-Power design Methodology proven with Taishan complements existing PPA/LP flows



Bridging **design methodology** gaps
Fast & safe implementation

User Guide
Low-Power SoC User Guide
for TSMC customers

Architectural Guidelines
Early Power Estimation with Figure of Merit

Architectural Guidelines
Specifying the Activity Control Unit

Architectural Guidelines
Defining Power Domains

Integration Guidelines & Rules
Implementing Power Domains

Bridging **EDA** gaps
Dynamic verifications to secure tape-out

SmartVision™
EDA solution for
Functional Verification to control the power domain mode transitions

SmartVision™ deliverables
- User Manual
- Tutorials
  - Getting Started
  - How to model a subsystem
  - Dhrystone Benchmarking
  - In-System Programming
  - In-Circuit Emulation

PowerVision™
EDA solution for
*Mode Transition Checks (**MTC**) & Noise Propagation Checks (**NPC**)*

PowerVision™ deliverables
- User Manual
- Tutorials
  - SMASH Getting Started
  - SLED Getting Started
  - PowerVision Getting Started
- Application Notes
  - How to extract Power Supply Noise Tolerance Template (PSNT2) of a Silicon IP

Complete Offering for Low-Power SoCs

55 nm ULP/ULP-eFlash
Ultra low-power technology platform
+
Reference Design Flows
PPA & Low-Power

Foundry sponsorship
+
Taishan demochip
+
Dolphin's complements

Technology and **Know-how** safe construct of an ultra-low power SoC

Silicon IP
Low-power & High-density
Foundation IPs
Feature IPs
Fabric IPs

EDA Solutions and methodology
Bridging the EDA gaps
Noise Propagation Checks
Mode Transition Checks

Low-power Design Methodology
Architectural Guidelines
Integration Guidelines and Rules

Design Services
SoC integration of uLP SoCs